JAYA KESHAVA CHANDRA KOTHA

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Objective

I aim to apply my strong foundation in software development, systems engineering, and hardware security to contribute to impactful engineering teams. I bring industry experience from AWS and advanced research in performance-driven threat detection, and I seek opportunities to build robust, scalable, and secure systems.

Education

University of California, Irvine, CA
Ph.D. in Electrical and Computer Engineering — Sept 2022 – Present
Advanced to Candidacy in June 2024, GPA: 4.0 (Estimated Dissertation: June 2027)

Research focuses on hardware-assisted runtime detection of microarchitectural attacks such as Spectre, Meltdown, and Rowhammer using hardware performance counters and machine learning. Current work explores adaptive frameworks and model generation techniques to enhance detection robustness and cross-platform scalability.

University of California, Irvine, CA
M.S. in Electrical and Computer Engineering — Sept 2018 – Dec 2019
Specializing in Computer Engineering, GPA: 4.0

Karunya University, Coimbatore, TN, India
B.Tech in Electronics and Communication Engineering — July 2013 – July 2017
CGPA: 8.78 (approx. 3.51 GPA)

Experience

University of California, Irvine, CA — Sept 2022 – Present
Lead Teaching Assistant / Teaching Assistant, Department of Electrical and Computer Engineering

- Lead TA for undergraduate and graduate-level courses, including Computer Architecture, Digital Systems, and software design.
- Guided students through complex hardware and mathematical concepts using inclusive, active-learning methods.
- Conducted lab sessions, graded coursework, and held office hours for over 100 students each quarter.
- Collaborated with course instructors to refine assignments and assessments for improved learning outcomes.

Amazon Web Services (AWS), Seattle, WA, USA — Mar 2020 – May 2022
Software Development Engineer

- Engineered scalable features for AWS Organizations, enabling seamless multi-account management for enterprise clients.
- Improved automation of account lifecycle operations, reducing manual provisioning overhead across millions of AWS accounts.
- Enhanced reliability and metadata integrity through cross-team collaboration—experience now leveraged in designing adaptive, large-scale detection frameworks.

Bharat Electronics, Hyderabad, India — May 2016 – June 2016
Student Intern

- Developed a 2–3 GHz frequency synthesizer using Phase-Locked Loop (PLL) and digital channel multiplexing.

Teaching Certifications

Mentoring Excellence Program (MEP), UC Irvine — Completed 2024
Five-week certificate program focused on developing effective mentoring practices for graduate students and postdoctoral scholars. Trained in providing academic, professional, and interpersonal support to mentees across diverse backgrounds.

Course Design Essentials (CDE), UC Irvine Completed 2024
Certificate program emphasizing evidence-based instructional design. Practiced backward course design by aligning learning objectives with assessments and teaching strategies.

Certificate in Teaching Excellence (CTE), UC Irvine In Progress (Expected 2025)
Comprehensive program by the Division of Teaching Excellence and Innovation (DTEI). Focuses on evidence-based pedagogy, peer observation, reflective teaching, and inclusive classroom strategies.

Publications & Research Works

Suganthi, E.C., Ashmiya, L., Jaya, K.C., Jeeva, P. "Monitoring and Control of Vital Parameters in Greenhouse using Internet of Things." *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, Vol. 8, Issue 9, pp. 849–859, July 2019.
Developed an IoT-based system for greenhouse parameter monitoring and control using sensors and cloud integration.

Jaya K., Gaudiot J. "A Data-Driven Approach Using Hardware Performance Counters to Detect Microarchitectural Attacks." In *Proceedings of the IEEE Symposium on Trusted Privacy and Security Architectures (STPSA 2025)*, co-located with *IEEE COMPSAC 2025*. DOI: 10.1109/COMPSAC65507.2025.00324.
Proposes a machine learning–based method leveraging hardware performance counters to detect microarchitectural attacks such as Spectre, aiming for adaptive runtime detection and cross-platform scalability.

Jaya Kotha, Jean-Luc Gaudiot. "Spectre Attack Detection: Cleaned Core Microarchitectural Counts (Intel & RPi, Background-Labeled)." *IEEE DataPort*, 2025. DOI: 10.21227/dqh5-n958.
Public dataset containing performance counter traces from Spectre attack executions and benign workloads across Intel and ARM platforms, facilitating reproducible research in runtime detection.

Research & Past Projects

Adaptive Runtime Detection of Microarchitectural Attacks Sep 2023 – Present
Designed a lightweight, hardware-assisted detection framework leveraging hardware performance counters to identify microarchitectural attacks such as Spectre and Rowhammer. Developed adaptive models to enhance detection robustness across Intel, ARM, and AMD architectures. Demonstrated high detection accuracy under diverse workloads without requiring hardware modifications or privileged access.

Past Projects

- **Cache Evaluation using Gem5** — Evaluated cache configurations on x86 using Splash2 benchmarks to analyze performance trade-offs.
- **Canny Edge Detector (SystemC and SpecC)** — Implemented real-time edge detection with pipelined parallelism for video processing.
- **Greenhouse Monitoring and Control (Reinforcement Learning)** — Used DHT11 and TCS34725 sensors with Raspberry Pi for adaptive climate control.
- **FabFix Full Stack Development** — Developed full-stack Java application with SQL backend, JavaScript/CSS frontend, and load-balanced microservices.
- **Greenhouse Monitoring System (Undergraduate Project)** — Built an IoT-based environmental monitoring system using Raspberry Pi and cloud data integration.

Additional Experience / Trainings

Bharat Electronics, Bangalore, KN, India Dec 2015
In-plant Training on Power Amplifiers and Synthesizers (2 weeks)

FPGA Implementation using Verilog Aug 2016 – Sep 2016
Add-on course: Implemented Verilog-based basic CPU and multiplexers

Academic Achievements

- Advanced to Ph.D. Candidacy, University of California, Irvine — June 2024
- Appointed Lead Teaching Assistant for core undergraduate courses, mentoring new TAs and supporting instructional improvement (2024–2025)
- Merit Certificate (3rd in Department), Karunya University, 2014

- Qualified Graduate Aptitude Test in Engineering (GATE), 2017

Skills

Programming Languages: Python, C, C++, Java, Embedded C, Verilog, SystemC, SpecC, HTML, CSS, JavaScript, MySQL

Machine Learning & Analysis: TensorFlow, scikit-learn, Pandas, NumPy, Matplotlib, PyTorch (basic)

Hardware & Tools: Linux `perf`, Gem5, Raspberry Pi 5 (ARM Cortex-A76), Intel Core i7/AMD Platforms, MATLAB, FPGA design

Development & Environment: Jupyter Notebook, Git, IntelliJ, VS Code, Raspbian OS, LaTeX

Other Skills: Data collection automation, cross-platform benchmarking, runtime detection model design, inclusive teaching

Languages Spoken: English (Fluent), Telugu (Fluent), Hindi (Fluent), Tamil (Conversational), Japanese (Conversational)